REMARKS

Applicant respectfully requests reconsideration of the prior art rejections set forth by the Examiner under 35 USC sections 102 and 103. Applicant respectfully submits that the prior art references of record, whether considered alone or in combination fail to either teach or suggest Applicants presently claimed invention.

Applicant also requests consideration of the references cited in the concurrently submitted information disclosure statement. Applicant notes that the closest references appears to be the references designated as X references in the corresponding search report and each appears to describe similar subject matter wherein chips that are mounted and secured to a common substrate have a protective material surrounding sides of the chips. However, this is far different than Applicants' invention as disclosed and now claimed wherein non-defective chips are advantageously formed into a pseudo wafer for the purpose of forming connections.

Applicants submit that neither the newly submitted references nor the ones previously asserted by the Examiner provide any teaching or suggestion whatsoever regarding this advance in the art. In order to underscore these distinctions, Applicants have modified the newly submitted independent claims to further require specify that the protective material adjacent the side surfaces of the semiconductor chip is cut to provide substantially vertical side walls of protective material formed adjacent the sides of the semiconductor chip. There is simply no teaching or suggestion whatsoever regarding this advance in the art.

More specifically, as described in the instant disclosure, a psudo wafer of non-defective chips is formed by securing the previously manufactured individual chips with resin formed adjacent the side surfaces of the chips so that a single wafer of non-defective chips may be further processed to advantageously provide common processing such as the manufacture of connections and the like as shown in the instant application. Thereafter the protective material adjacent the side surfaces of the semiconductor chip is cut to provide substantially vertical side walls of protective material formed adjacent the sides of the semiconductor chip. None of the references of record teach or suggest this advance in the art.

In light of the foregoing, Applicant request that the Examiner now allow all claims in the application.

Respectfully submitted,

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(Reg. #37,607)

Robert J. Depke
HOLLAND & KNIGHT LLC
131 S. Dearborn, 30th Floor
Chicago, Illinois 60603
Tel: (312) 263-3600
Attorney for Applicant

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail on February 27, 2004 in an envelope addressed to:

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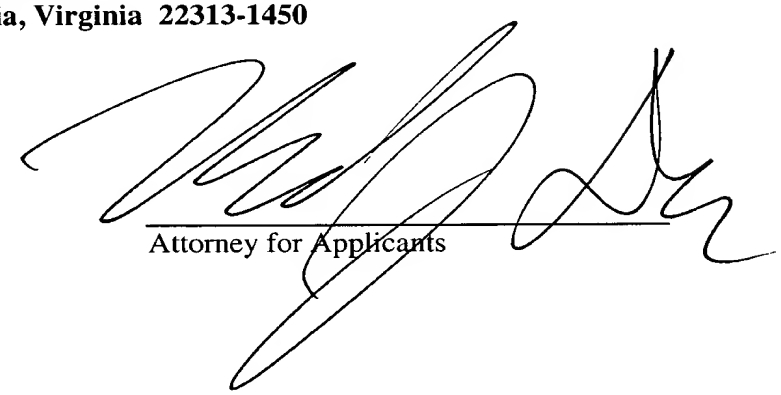

Attorney for Applicants